9th Conference on Reversible Computation

The Pride Plaza Hotel, Kolkata, India

July 6-7, 2017

July 5, 2017 (Wednesday)

9:30 – 17:30 Summer School on Reversible and Quantum Computing

16:00 – 18:00 Registration for RC-2017

July 6, 2017 (Thursday)

8:00 – 9:00 Registration for RC-2017

9:00 – 9:15 Inauguration

9:15 – 10:15 **Invited Talk 1**

Relating the Limits of Computational Reversibility to Emergence
Kalyan S. Perumalla

10:15 – 10:45 Tea / Coffee Break

10:45 – 12:35 **Session I (3R + 1S) Foundations**

Foundations of Generalized Reversible Computing
Michael P. Frank

Reversible Nondeterministic Finite Automata
Markus Holzer and Martin Kutrib

Capacitive-based Adiabatic Logic
Ayrat Galisultanov, Yann Perrin, Hervé Fanet and Gaël Pillonnet

Implementing Reversible Object-Oriented Language Features on Reversible Machines
Tue Haulund, Torben Mogensen and Robert Glück

12:35 – 13:35 Lunch Break

13:35 – 15:25 **Session II (3R + 1S) Reversible Circuits I**

Designing Parity Preserving Reversible Circuits
Goutam Paul, Anupam Chattopadhyay and Chander Chandak

REVS: A tool for space-optimized reversible circuit synthesis
Alex Parent, Martin Roetteler and Krysta Svore

Optimizing the Reversible Circuits using Complementary Control Line Transformation
Sai Phaneendra P, Chetan Vudadha and M.B. Srinivas

Towards VHDL-based Design of Reversible Circuits
Zaid Al-Wardi, Robert Wille and Rolf Drechsler

15:25 – 15:55 Tea / Coffee Break

15:55 – 17:15 **Session III (2R + 1S) Reversible Circuits II**

Test Pattern Generation Effort Evaluation of Reversible Circuits
Abhoy Kole, Robert Wille, Kamalika Datta and Indranil Sengupta

An ESOP Based Cube Decomposition Technique for Reversible Circuits
Sai Phaneendra P, Chetan Vudadha and M.B. Srinivas

Controlled and Uncontrolled SWAP Gates in Reversible Logic Synthesis
Md Asif Nashiry, Mozammel H.A. Khan and Jacqueline E. Rice

18:00 – 21:30 **Cultural Function + Banquet Dinner**

July 7, 2017 (Friday)

9:15 – 10:15 **Invited Talk 2**

Tools for Quantum and Reversible Circuit Compilation
Martin Roetteler

10:15 – 10:45 Tea / Coffee Break

10:45 – 12:35 **Session IV (3R + 1S) Quantum Circuits and Testing**

Exact Global Reordering for Nearest Neighbor Quantum Circuits Using A*
Alwin Zulehner, Stefan Gasser and Robert Wille

Improved Decomposition of Multiple-Control Ternary Toffoli Gates using Muthukrishnan-Stroud Quantum Gates
P. Mercy Nesa Rani, Abhoy Kole, Kamalika Datta and Indranil Sengupta

A method to reduce resources for quantum error correction
Ritajit Majumdar, Saikat Basu and Susmita Sur-Kolay

Automatic Test Pattern Generation for Multiple Missing Gate Faults in Reversible Circuits
Anmol Prakash Surhonne, Anupam Chattopadhyay and Robert Wille

12:35 – 13:35 Lunch Break

13:35 – 15:00 **Session V (2R + 1S) Quantum Circuits**

Efficient Construction of QMDDs for Irreversible, Reversible, and Quantum Functions
Philipp Niemann, Alwin Zulehner, Robert Wille and Rolf Drechsler

Improving Synthesis of Reversible Circuits: Exploiting Redundancies in Paths and Nodes of QMDDs
Alwin Zulehner and Robert Wille

Design of Efficient Quantum Circuits using Nearest Neighbor Constraint in 2D Architecture
Leniency Marbaniang, Abhoy Kole, Kamalika Datta and Indranil Sengupta

15:00 – 15:30 Tea / Coffee Break

15:30 – 16:15 **Open Discussion Session**

16:15 – 16:30 Closing Session

17:00 – 21:30 **Social Program + Dinner**

R: Regular paper (16 proceedings pages; 30 minutes total presentation time)

S: Short paper (6 proceedings pages; 20 minutes total presentation time)