Summer School :: July 5, 2017 (Wednesday)

9:30–10:15	Reversible Logic: From Foundations to Frontiers *Bhargab Bhattacharyya, Indian Statistical Institute Calcutta, India*
10:15–11:00	Algebra for Reversible Logic Circuits *M. H. A. Khan, East West University, Dhaka, Bangladesh*
11:30–12:15	Adiabatic Circuits *Michael P. Frank, Sandia National Laboratories, USA*
12:15–13:00	Reversible Programming Models and Paradigms *Kalyan S. Perumalla, Oak Ridge National Laboratory, USA*
13:45–15:30	Reversible Logic Synthesis and RevKit *Mathias Soeken, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland*
16:00–16:45	Reversible Circuit Testing *Debesh Das, Jadavpur University, Kolkata, India*
16:45–17:45	Applications of Reversible Circuits and Directions for Future Work *Robert Wille, Johannes Kepler University Linz, Austria*

Conference Day 1 :: July 6, 2017 (Thursday)

9:00–9:15	**Inauguration**
9:15–10:15	**Invited Talk 1** Relating the Limits of Computational Reversibility to Emergence *Kalyan S. Perumalla, Oak Ridge National Laboratory, Tennessee, USA*
10:45–12:35	**Session I: Foundations** • Foundations of Generalized Reversible Computing, *M. P. Frank* • Reversible Nondeterministic Finite Automata, *M. Holzer, M. Kutrib* • Capacitive-based Adiabatic Logic, *A. Galisultanov, Y. Perrin, H. Fanet, G. Pillonnet* • Implementing Reversible Object-Oriented Language Features on Reversible Machines, *T. Haulund, T. Mogensen, R. Glück*
13:35–15:25	**Session II: Reversible Circuits I** • Designing Parity Preserving Reversible Circuits, *G. Paul, A. Chattopadhyay, C. Chandak* • REVS: A tool for space-optimized reversible circuit synthesis, *A. Parent, M. Roetteler, K. Svore* • Optimizing the Reversible Circuits using Complementary Control Line Transformation, *Sai Phaneendra P, C. Vudadha and M.B. Srinivas* • Towards VHDL-based Design of Reversible Circuits, *Z. Al-Wardi, R. Wille, R. Drechsler*
15:55–17:15	**Session III: Reversible Circuits II** • Test Pattern Generation Effort Evaluation of Reversible Circuits, *A. Kole, R. Wille, K. Datta, I. Sengupta* • An ESOP Based Cube Decomposition Technique for Reversible Circuits, *Sai Phaneendra P, C. Vudadha, M.B. Srinivas* • Controlled and Uncontrolled SWAP Gates in Reversible Logic Synthesis, *M.A. Nashiry, M.H.A. Khan, J. E. Rice*
18:00–21:30	**Banquet Speech** :: *Gerhard Dueck, University of New Brunswick, Canada* **Cultural Function + Banquet Dinner**

Conference Day 2 :: July 7, 2017 (Friday)

9:15–10:15	**Invited Talk 2** Tools for Quantum and Reversible Circuit Compilation *Martin Roetteler, Microsoft Research Redmond, USA*
10:45–12:35	**Session IV: Quantum Circuits and Testing** • Exact Global Reordering for Nearest Neighbor Quantum Circuits Using A*, *A. Zulehner, S. Gasser, R. Wille* • Improved Decomposition of Multiple-Control Ternary Toffoli Gates using Muthukrishnan-Stroud Quantum Gates, *P.M.N. Rani, A. Kole, K. Datta, I. Sengupta* • A method to reduce resources for quantum error correction, *R. Majumdar, S. Basu, S. Sur-Kolay* • Automatic Test Pattern Generation for Multiple Missing Gate Faults in Reversible Circuits, *A.P. Surhonne, A. Chattopadhyay, R. Wille*
13:35–15:00	**Session V: Quantum Circuits** • Efficient Construction of QMDDs for Irreversible, Reversible, and Quantum Functions, *P. Niemann, A. Zulehner, R. Wille, R. Drechsler* • Improving Synthesis of Reversible Circuits: Exploiting Redundancies in Paths and Nodes of QMDDs, *A. Zulehner, R. Wille* • Design of Efficient Quantum Circuits using Nearest Neighbor Constraint in 2D Architecture, *L. Marbaniang, A. Kole, K. Datta, I. Sengupta*
15:30–16:15	**Open Discussion Session**
16:15–16:30	**Closing Session**